The advances in strain engineering must be supported by improvements in local strain characterization techniques to address the simulation, design and fabrication challenges faced by the semiconductor industry. Though TEM is the method of choice for nanoscale measurement of strain, the existing techniques suffer from serious limitations such as the poor strain sensitivity of $10^{-3}$ for high-resolution imaging or the difficulty of using dark field electron holography to analyze silicon-on-insulator (SOI) devices due to the miscut between the region of interest and the substrate. Recently, Rouvière et al. [1] introduced the use of precession electron diffraction (PED) for strain measurement with 1 nm spatial resolution and $2 \times 10^{-4}$ sensitivity. In this study we demonstrate that strain can be precisely measured by PED in aggressively scaled devices. For this purpose, PED is compared to geometrical phase analysis (GPA) on HAADF STEM images and Finite Element simulations on 11.5-nm-wide channel SOI device and sub-10 nm SiGe nanowire.

The HAADF images and PED patterns have been acquired on a FEI Titan Ultimate microscope equipped with two Cs-correctors and an X-FEG source operated at 200 kV. The PED patterns have been recorded on a 2k x 2k Gatan CCD camera using a precession speed of 0.1 s, a semi-convergence angle of 2.4 mrad, a precession angle of 12.7 mrad and a beam size of ~ 2 nm (measured on the sample with the precession activated). For both techniques: (i) the deformation is measured relative to the Si substrate, (ii) non-pertinent areas of strain mappings are removed based on either the amplitude image of the inverse filtered Fourier transform for GPA or the virtual HAADF image computed from diffraction patterns for PED.

As seen from Figs. 2(a-c), the strain ($\varepsilon_{002}$ and $\varepsilon_{220}$ along the growth and in-plane directions, respectively) and rotation ($\theta$) maps measured by PED and GPA on the SOI device shown in Fig. 1(a) are in good agreement. They both give evidence of a fully relaxed state. More importantly, the strain profiles (Fig. 2(d)) measured along the channel prove that the noise is significantly reduced using PED, allowing the strain state in small areas, e.g. source-drain (S/D), to be precisely determined. The higher strain level measured in S/D is consistent with the Ge enrichment in S/D measured by EDX (Figs. 1(c-d)). Figs. 3(e-f) demonstrate that high precision and high spatial resolution strain distributions can be acquired by PED on a sub-10 nm SiGe nanowire. As seen from Figs. 3(b-c), GPA applied to the same device provides mappings composed of high strain field fluctuations which make the interpretation of the strain state in nanowires difficult.


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Fig. 1: (a) HAADF STEM image of the SOI device, (b) magnified image indicated in (a) by the blue rectangle, (c) Ge and (d) Si EDX mappings (see the color legends for the concentration in at. %)

Fig. 2: (a-c) Comparison between the different strain and rotation maps measured by PED and GPA on the SOI device shown in Fig. 1 (the substrate is not shown for better visualization), (d) strain profiles acquired along the channel and S/D. Note the significant noise reduction using PED.

Fig. 3: (a) HAADF STEM and (d) virtual HAADF computed from the PED patterns acquired on the SiGe nanowire; (b-c) GPA and (e-f) PED measured strain mappings.